

WHAT IS CLAIMED IS:

- 1 1. A method for transferring data in a data processing unit comprising:
2 receiving a first address;
3 if the first address contains a predetermined address component, then
4 producing a second address and accessing a memory location at the second address; and
5 if the first address does not contain the predetermined address component,
6 then accessing a memory location at the first address,
7 the first address comprising a plurality of address bits, wherein the
8 predetermined address component comprises less than all of the address bits of the first
9 address,
10 the first address and the second address having a common address component.
- 1 2. The method of claim 1 wherein the predetermined address component
2 comprises the high order byte of the first address.
- 1 3. The method of claim 1 further comprising executing a virtual machine
2 in a first page of an address space of the data processing unit, the first address being an
3 address in the first page, wherein the second address is an address in another page of the
4 address space of the data processing unit.
- 1 4 The method of claim 1 wherein an address space of the data processing
2 unit comprises a plurality of pages, the first address being an address in a first page, the
3 second address being in an address in a second page that is different from the first page.
- 1 5. A data processor comprising a memory management unit for handling
2 addresses, the memory management unit comprising:
3 address input lines for presenting an input address;
4 address translation logic coupled to at least some of the address input lines;
5 and
6 address output lines coupled to the address translation logic for presenting an
7 output address,
8 the address translation logic operable to receive a first input address from the
9 address input lines and to generate a first output address on the address output lines that is
10 different from the first input address if a portion of the first input address contains a
11 predetermined value.

1 6. The data processor of claim 5 wherein the address translation logic is
2 further configured to detect a predetermined value present in the high order bits of the input
3 address.

1 7. The data processor of claim 5 wherein the memory management unit
2 further comprises a translation table, the translation table comprising M-bit values, the
3 translation table addressed by an N-bit value, where $M > N$, wherein the translation table
4 produces one of the M-bit values based on N lines of the address input lines, wherein the M-
5 bit value produced is used in M lines of the address output lines.

1 8. The data processor of claim 7 wherein the remaining lines in the
2 address output lines come from the address input lines.

1 9. A method for transferring data in a data processing unit comprising:
2 accessing a first value from a first data storage component of the data
3 processing unit;

4 combining the first value with a base address to produce a first address, the
5 base address representative of an area in a memory;

6 accessing a second value from a second data storage component of the data
7 processing unit;

8 accessing a third value from a third data storage component of the data
9 processing unit;

10 combining the second value with a value stored in a location in the memory
11 indicated by the first address to produce a fourth value;

12 comparing the third value with the fourth value to produce a comparison
13 result; and

14 based on the comparison result, either accessing the memory beginning at a
15 location indicated by a second address or performing an exception operation, the second
16 address being computed from the base address.

1 10. The method of claim 9 further including one or more steps of storing
2 the first value in the first data storage component, storing the second value in the second data
3 storage component, and storing the third value, wherein the one or more steps of storing are
4 performed only at the time the data processing unit is initialized.

1 11. The method of claim 9 wherein one or more of the first value, the
2 second value, and third value is stored respectively in the first data storage component, the
3 second data storage component, and the third data storage component in a non-volatile
4 manner.

1 12. The method of claim 9 further comprising loading one or more of the
2 first data storage component, the second data storage component, and the third data storage
3 component respectively with the first value, the second value, and third value.

1 13. The method of claim 9 wherein the second address is computed based
2 on the base address and an offset value.

1 14. The method of claim 13 wherein the second address is computed by
2 adding together the base address and the offset value.

1 15. The method of claim 9 wherein the exception operation comprises
2 accessing content of a fourth data storage component, wherein subsequent processing by the
3 data processing unit continues from instructions beginning at a location in memory computed
4 based on the content of the fourth data storage component.

1 16. The method of claim 15 wherein the location in memory where
2 subsequent processing continues is computed by adding the content of the fourth data storage
3 component with an offset value.

1 17. The method of claim 9 wherein the area in memory represents a data
2 object.

1 18. The method of claim 9 wherein the step of accessing is a step of
2 copying the accessed content to another area in the memory.

1 19. The method of claim 9 wherein the step of accessing is a step of
2 writing information to the accessed content.

1 20. The method of claim 9 wherein the first address is produced by adding
2 together the first value and the base address.

1 21. A data processing unit comprising:

2 a memory;
3 instruction decoder logic for producing control signals in response to decoding
4 program instructions;
5 data processing logic coupled to receive the control signals and configured to
6 perform logic operations in accordance with the control signals;
7 an instruction register coupled to the memory and to the instruction decoder,
8 the instruction register operable to store an instruction to be decoded;
9 a program counter operable to store an address of an instruction to be decoded;
10 a vector address data area for storing a vector address;
11 a first data area for storing a first value;
12 a second data area for storing a second value; and
13 a third data area for storing a third value,
14 the instruction decoder configured to assert first control signals in response to
15 decoding a first instruction,
16 the data processing logic, in response to the first control signals, configured to:
17 combine the first value with a first operand contained in the first instruction to
18 produce a first address;
19 combine the second value with a value stored in the memory at a location
20 indicated by the first address to produce a fourth value;
21 compare the third value with the fourth value to produce a comparison result;
22 and
23 based on the comparison result, either access the memory beginning at a
24 location indicated by a second address or update the program counter with an address based
25 on the vector address, the second address being computed from the first operand.

1 22. The data processing unit of claim 21 wherein the memory is a re-
2 programmable, non-volatile memory.

1 23. The data processing unit of claim 21 wherein the memory is one of an
2 EEPROM (electrically erasable programmable read-only memory) and flash memory.

1 24. The data processing unit of claim 21 wherein the data processing logic,
2 in response to initialization of the data processing unit, is further configured to load data into
3 one or more of the vector address data area, the first data area, the second data area, and the
4 third data area.

1 25. The data processing unit of claim 21 wherein one or more of the vector
2 address data area, the first data area, the second data area, and the third data area comprise
3 non-volatile memory.

1 26. The data processing unit of claim 25 wherein the non-volatile memory
2 is one of EEPROM (electrically erasable programmable read-only memory) or PROM
3 (programmable read-only memory).

1 27. The data processing unit of claim 21 wherein one or more of the vector
2 address data area, the first data area, the second data area, and the third data area comprise
3 hard-wired logic.

1 28. The data processing unit of claim 21 wherein the instruction decoder is
2 further configured to assert a second set of control signals in response to decoding a second
3 instruction, the data processing logic, in response to the second control signals, is further
4 configured to load data into one or more of the vector address data area, the first data area,
5 the second data area, and the third data area, the data contained in the second instruction.

1 29. The data processing unit of claim 21 wherein the data processing logic,
2 in response to the first control signals, is further configured to combine the first operand with
3 a second operand contained in the first instruction to produce the second address.

1 30. The data processing unit of claim 29 wherein the first operand and the
2 second operand are summed to produce the second address.

1 31. A memory access method in a data processing unit comprising re-
2 programmable non-volatile memory, the method comprising:
3 detecting a write operation to an area in the re-programmable non-volatile
4 memory;
5 determining a caching location which identifies an area of memory in a
6 dynamic memory to which data to be written by the write operation can be cached, the area of
7 memory identified by the caching location referred to as a caching area; and
8 writing the data to the caching area instead of writing the data to the area in
9 the re-programmable non-volatile memory,

10 wherein the caching area is associated with the area in the re-programmable
11 non-volatile memory.

1 32. The method of claim 31 wherein the step of determining a caching
2 location comprises:
3 determining if the data can be stored in the dynamic memory, and if not then:
4 identifying one or more memory locations in the dynamic memory;
5 and
6 writing content in the one or more memory locations to the re-
7 programmable non-volatile memory; and
8 providing an address in the dynamic memory as the caching location in the
9 area of memory.

1 33. The method of claim 32 wherein the step of determining a caching
2 location in the dynamic memory is limited to determining a caching location in a segment of
3 the dynamic memory.

1 34. The method of claim 31 further including detecting a second write
2 operation to the area in the re-programmable non-volatile memory and writing the data
3 associated with the second write operation to the area of memory identified by the caching
4 location instead of writing the data to the area in the re-programmable non-volatile memory.

1 35. The method of claim 31 further including detecting a second write
2 operation to a second area in the re-programmable non-volatile memory, determining if there
3 is a caching area in the dynamic memory that is associated with the second area and if there is
4 then writing data associated with the second write operation to the caching area associated
5 with the second area.

1 36. The method of claim 31 wherein an address space of the re-
2 programmable non-volatile memory is equal to or greater than an address space of the
3 dynamic memory.

1 37. The method of claim 32 wherein the step of identifying one or more
2 memory locations is based on the size of the data.

1 38. The method of claim 32 wherein the step of identifying one or more
2 memory locations is based on contents of the data.

1 39. The method of claim 38 wherein the step of identifying one or more
2 memory locations includes applying a hash function on the data to produce a hash result, the
3 one or more locations determined based on the hash result.

1 40. The method of claim 31 wherein the re-programmable non-volatile
2 memory is one of an EEPROM (electrically erasable programmable read-only memory) and a
3 flash memory.

1 41. The method of claim 31 further including obtaining an address range
2 which defines the area of memory in the dynamic memory.

1 42. The method of claim 31 further including detecting a read operation
2 from the re-programmable non-volatile memory and reading the re-programmable non-
3 volatile memory to effect the read operation.

1 43. The method of claim 31 further including detecting a read operation
2 from the re-programmable non-volatile memory and reading one or more memory locations
3 from the area of memory in the dynamic memory to effect the read operation.

1 44. A data processing unit comprising:
2 a bus for accessing a dynamic memory;
3 a re-programmable non-volatile memory;
4 memory access logic operatively coupled to the memory bus and to the re-
5 programmable non-volatile memory; and
6 processor logic operatively coupled to the memory access logic to transfer
7 data with the dynamic memory via the memory bus and to transfer data with the re-
8 programmable non-volatile memory,
9 the memory access logic configured to detect a write operation to the re-
10 programmable non-volatile memory,
11 the processor logic configured to respond to the memory access logic
12 detecting the write operation and to:

13 identify a caching location in the area of memory wherein data to be
14 written by the write operation can be cached; and
15 store the data in the area of memory identified by the caching location.

1 45. The data processing unit of claim 44 wherein the memory access logic
2 is further configured to:
3 determine if the data can be stored in the area of memory; and
4 provide an address in the area of memory as the caching location in the area of
5 memory,
6 wherein if it is determined that the data cannot be stored in the area of
7 memory, then:
8 identify one or more memory locations in the area of memory; and
9 write content in the one or more memory locations to the re-programmable
10 non-volatile memory,
11 wherein the one or more memory locations are available for caching a write
12 operation.

1 46. The data processing unit of claim 44 wherein an address space of the
2 re-programmable non-volatile memory is equal to or greater than an address space of the
3 dynamic memory.

1 47. The data processing unit of claim 44 wherein the re-programmable
2 non-volatile memory is one of an EEPROM (electrically erasable programmable read-only
3 memory) and a flash memory.

1 48. The data processing unit of claim 44 wherein the dynamic memory is a
2 random access memory.

1 49. The data processing unit of claim 44 wherein the memory access logic
2 is further configured to detect a read operation from the re-programmable non-volatile
3 memory and to effect a read operation therefrom.

1 50. The data processing unit of claim 44 wherein the memory access logic
2 is further configured to detect a read operation from the re-programmable non-volatile
3 memory and to access the area in memory in the dynamic memory to effect the read
4 operation.

1 51. A memory access method comprising:
2 detecting a write operation to a re-programmable non-volatile memory; and
3 if a destination address associated with the write operation is within a first
4 range of addresses, then performing a fast write operation of data associated with the write
5 operation to the re-programmable non-volatile memory.

1 52. The method of claim 51 wherein the first range of addresses spans the
2 entire address space of the re-programmable non-volatile memory.

1 53. The method of claim 51 wherein if the destination address is not within
2 the first range of addresses, then performing a slow write operation of the data to the re-
3 programmable non-volatile memory.

1 54. The method of claim 51 wherein the first range of addresses spans a
2 range of addresses less than the address space of the re-programmable non-volatile memory.

1 55. The method of claim 51 wherein the step of performing a fast write
2 operation is performed if the destination address falls within any of a plurality of ranges of
3 addresses.

1 56. A memory access method comprising:
2 detecting a write operation to a non-volatile memory;
3 determining an access mode;
4 if the access mode is a first mode, then performing a fast write operation of
5 data associated with the write operation to the non-volatile memory;
6 if the access mode is a second mode, then performing a slow write operation
7 of the data associated with the write operation; and
8 if the access mode is a third mode, then:
9 if the destination address associated with the write operation is within a
10 first range of addresses, then performing a fast write operation of the data associated
11 with the write operation to the non-volatile memory;
12 if the destination address is not within the first range of addresses, then
13 performing a slow write operation of the data to the non-volatile memory; and
14 if the access mode is a fourth mode, then:

15 determining a caching location which identifies an area of memory in a
16 dynamic memory to which data to be written by the write operation can be cached, the
17 area of memory identified by the caching location referred to as a caching area; and
18 writing the data to the caching area instead of writing the data to the
19 area in the non-volatile memory,
20 wherein the caching area is associated with the area in the non-volatile
21 memory.

1 57. A memory control logic for accessing a re-programmable non-volatile
2 memory comprising:

3 write detection logic to determine when a write operation to the memory is
4 being performed;

5 address detection logic configured to indicate a detected address when a
6 destination address associated with a write operation falls within a first range of addresses;
7 and

8 write-control logic operatively coupled to the address detection logic and
9 configured to perform a shallow-write operation of data associated with the write operation
10 when the address detection logic indicates a detected address.

1 58. The memory control logic of claim 57 further comprising a first
2 address register and a second address register, wherein the first range of addresses comprises
3 data stored in the first and second address registers.

1 59. The memory control logic of claim 57 further comprising a plurality of
2 register pairs, each register pair representative of a range of addresses in an address space of
3 the memory, wherein the address detection logic is further configured to indicate a detected
4 address when the destination address falls within any of the ranges of addresses represented
5 by the plurality of register pairs.

1 60. The memory control logic of claim 57 wherein the re-programmable
2 non-volatile memory is one of an EEPROM (electrically erasable programmable read-only
3 memory) and a flash memory.

1 61. A memory control logic for accessing a re-programmable non-volatile
2 memory comprising write detection logic to determine when a write operation to the memory

3 is being performed and write-control logic configured to perform a shallow-write operation of
4 data associated with the write operation.

1 62. The memory control logic of claim 61 wherein the re-programmable
2 non-volatile memory is one of an EEPROM (electrically erasable programmable read-only
3 memory) and a flash memory.

1 63. A memory access method for accessing a re-programmable non-
2 volatile memory comprising:

3 detecting a write operation to the re-programmable non-volatile memory, the
4 write operation having an associated destination address and associated one or more data to
5 be written to the re-programmable non-volatile memory;

6 determining an operating mode;

7 if the operating mode indicates a first mode of operation, then:

8 performing a partial write operation of each datum to the re-
9 programmable non-volatile memory, if the destination address is within a first range
10 of addresses; and

11 performing a full write operation of each datum to the re-
12 programmable non-volatile memory, otherwise;

13 if the operating mode indicates a second mode of operation, then performing a
14 full write operation of each datum to the re-programmable non-volatile memory;

15 if the operating mode indicates a third mode of operation, then performing a
16 partial write operation of each datum to the re-programmable non-volatile memory; and

17 if the operating mode indicates a fourth mode of operation, then:

18 determining a caching location which identifies an area of memory in a
19 dynamic memory where the data can be cached; and

20 writing the data in the area of memory identified by the caching
21 location instead of writing to the re-programmable non-volatile memory.

1 64. The method of claim 63 wherein the re-programmable non-volatile
2 memory is one of an EEPROM (electrically erasable programmable read-only memory) and a
3 flash memory.